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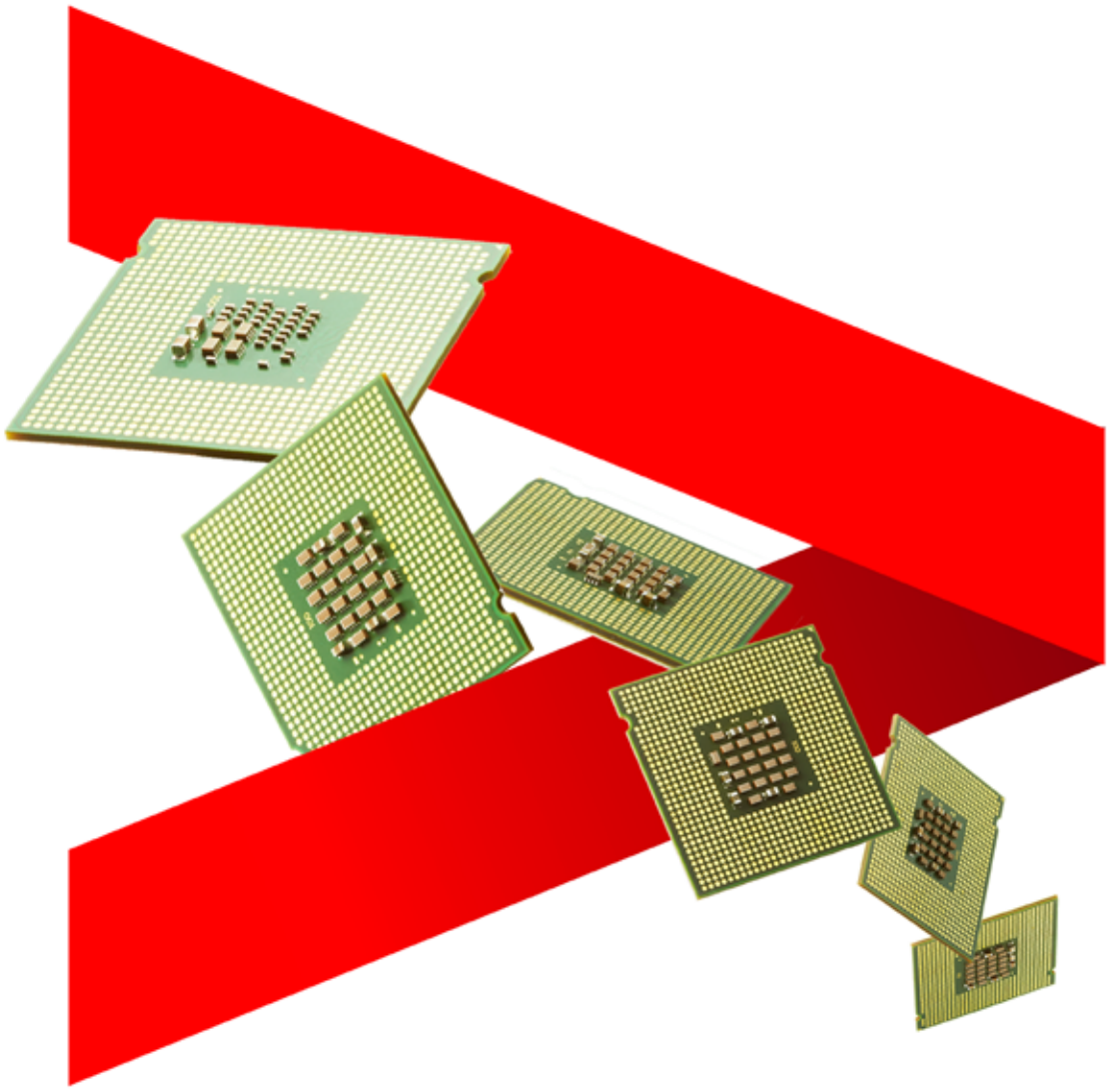
MOORE... OR LESS?



SYED ALAM | GREG DOUGLASS

In 1965, Dr. Gordon Moore suggested that semiconductor companies would double the number of transistors in an integrated circuit every two years. For 50 years—or about 40 years longer than Dr. Moore had envisioned—they have done just that. Moore's Law has become the guiding principle for the industry.

Today, it's becoming harder for semiconductor companies to justify the use of Moore's Law as a viable tool for business growth and sustained competitiveness. That's because the cost associated with increasing transistor density is rising exponentially, while average sales prices are flat or declining.

In this high-cost/low-return environment, semiconductor companies face tough choices. And some are realizing that achieving competitive agility means knowing when to say "less is more."

A BALANCING ACT

Since Moore's Law was first observed, semiconductor manufacturers steadily and painstakingly reduced the critical dimensions of transistor components. These advances allowed them to free up wafer real estate for additional die, which not only boosted processing power, but also the semiconductor industry's profitability.

Today, there is no guarantee that the rewards associated with advanced chip development will outweigh the costs. Semiconductor companies must think carefully about where—and whether—to invest in advanced chip production. They also need to balance several opposing forces.

Historically, the opportunity to offer the latest node technologies was appealing because the cost to do so was reasonable and the market demand was high. And while demand for advanced solutions remains high, the market dynamics have changed.

TECHNOLOGY VS. SUPPLY

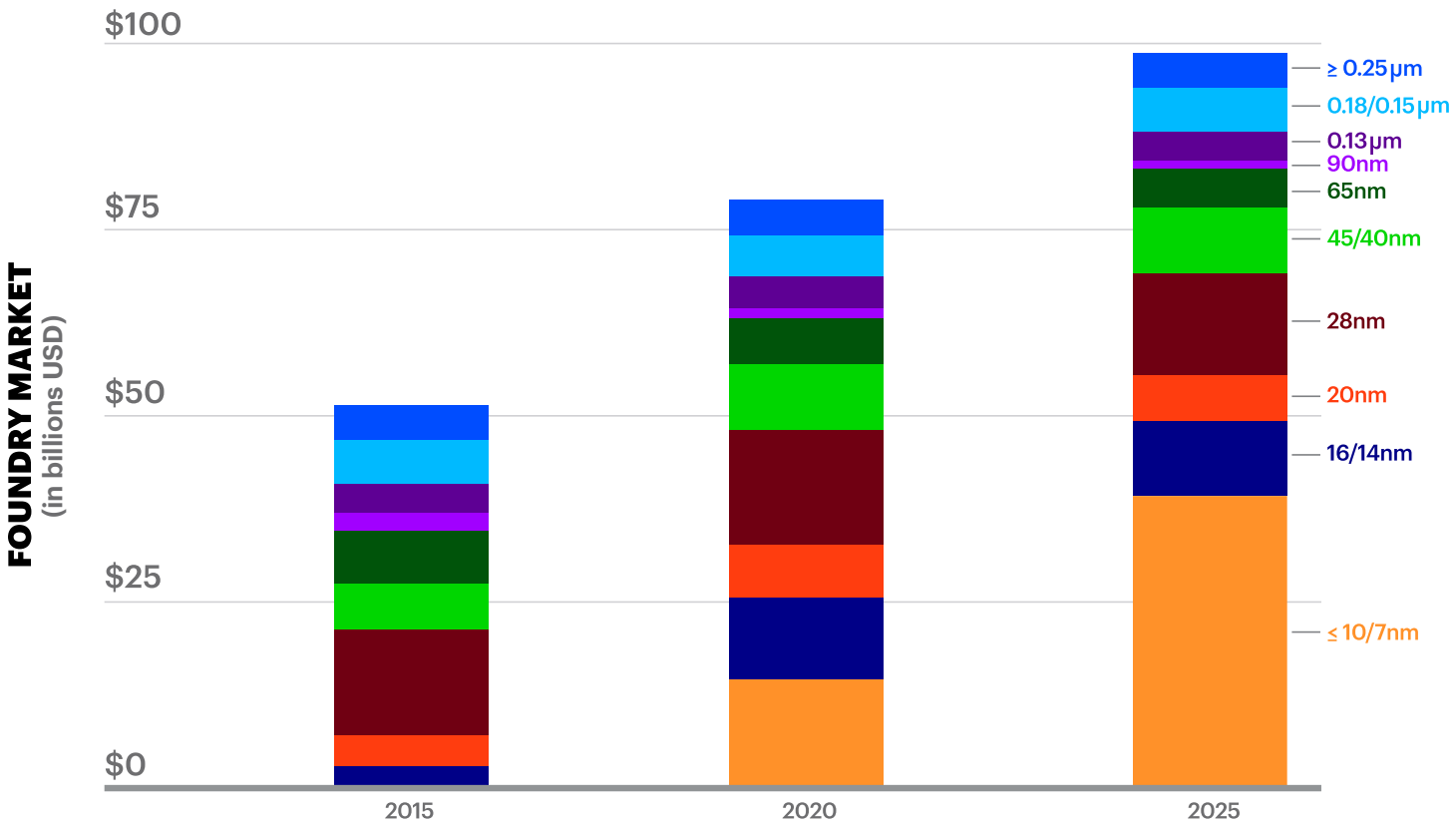
In 1971, Intel was the only semiconductor company capable of producing a commercially viable technology node at 10µm.[1] Today, the industry comprises many players capable of producing technology of all process sizes—from the original 10µm to the popular 180nm–130nm range, down to the highly advanced 28nm and 14nm nodes.

Because nodes in the 28nm to 14nm range are already so densely packed, it's much harder and more complex to reduce the critical dimensions of transistor components any further. It's also exponentially more expensive. Creating the next generation of ultra-dense chips requires more manufacturing cycle time, additional manufacturing steps and additional headcount.

Fortunately, many semiconductor customers don't need to transition to the newest generation of nodes. A number of common devices, circuits and services such as Wi-Fi and

Bluetooth still rely on 28nm or even older nodes.[2] While newer, more advanced nodes—especially with process sizes of 10nm or less—will account for greater foundry market share in the years ahead, the market share for older nodes is expected to remain generally consistent (see Figure 1). That is due to several factors, including a large IP portfolio for 28nm-enabled products, abundant expertise in designing for older nodes, and wafer processes that require less power consumption and cost. As the market for 10nm and smaller process technologies is expected to grow from $14.8 billion in 2020 to $39 billion in 2025, these newer nodes will not cannibalize older ones. In an expanding market, ≥28nm nodes will reveal remarkable staying power.[3]

Figure 1. Projected foundry market by node feature dimensions, 2015-2025.



Source: Dr. Handel Jones (International Business Strategies), "Semiconductor Industry from 2015 to 2025," SEMI, August 4, 2015.

Semiconductor companies have an important choice to make. They can move ahead with production of ultra-dense (≤10nm) nodes, but will likely find their supply restricted by design costs and limited manufacturing capacity. Or they can maintain a steady supply of 20nm-65nm nodes at a reasonable cost. With this option, they run the risk of potentially losing customers that want more advanced technology. In an ideal world, they will not choose one strategy over the other. They will wisely balance their investments across the old and new technology landscape.

GROWTH VS. PROFITABILITY

Achieving competitive agility requires an integrated focus on both growth and profitability. For semiconductor companies, finding the right balance can be tough. The cost of producing 45nm nodes vs. 65nm nodes is only marginally higher. But for newer nodes, design costs have grown exponentially—by 1300 percent from 65nm to 10nm. To put that in perspective, annual design costs for 65nm chips is well below $50 million. At 7nm, chip component design costs are expected to exceed $400 million. At 5nm, the cost tops $600 million.[4]

In the past, semiconductor companies could justify high initial design investments because the cost of designing and manufacturing newer nodes came down over time, as yield and production quality ramped up. Each successive generation of technology took advantage of lower manufacturing costs than the previous generation. That phenomenon is no longer occurring (see Figure 2). The two-year projected average cost (2017-2019) per thousand gates of 20nm and 16nm technology nodes are actually higher than the 28nm cost.[5] This suggests there is little potential upside for manufacturers to invest in the more expensive and more complex 20nm-16nm nodes.

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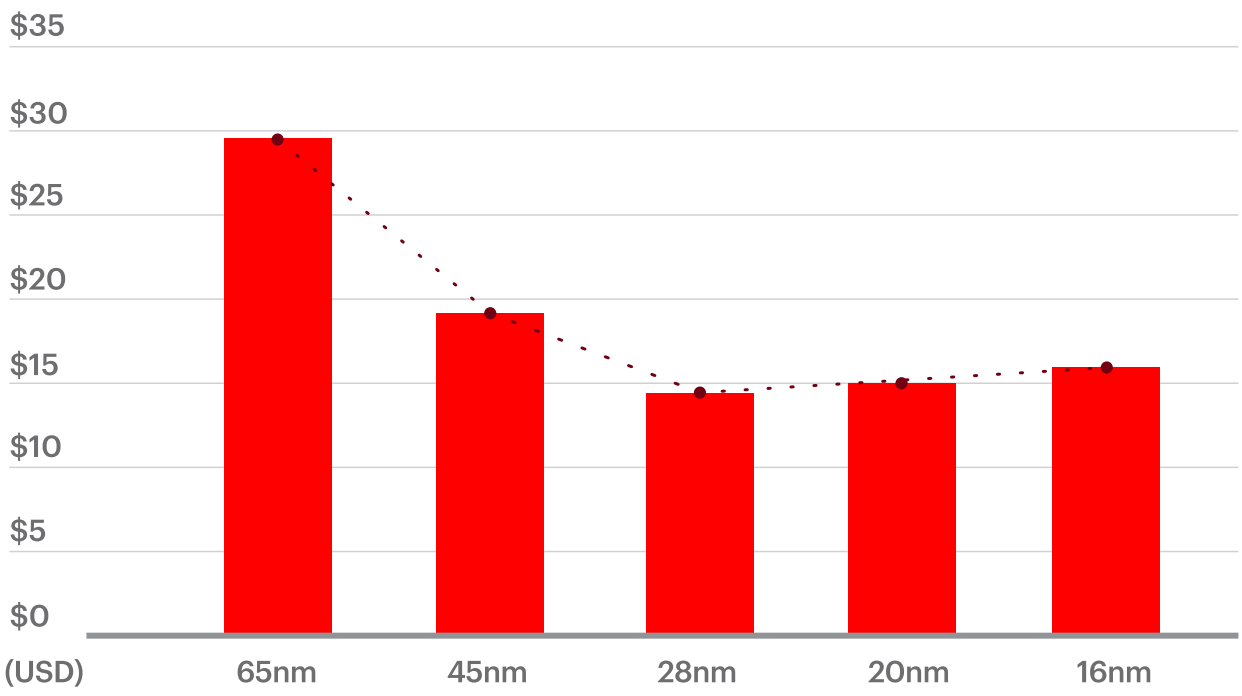
Companies need to realize they can no longer rely on technological advancements from Moore's Law to drive manufacturing profitability. Moving to advanced node design will likely deliver growth in certain sectors demanding denser nodes, but not profit. The rising tide of increased chip density is no longer an industry standard, and companies must identify other opportunities for their older, more economical technologies.

Figure 2. Projected average cost per gate of newer-node transistors are no longer falling, 2017-2019.



Source: Accenture Strategy analysis.

QUALITY VS. COST

As companies pack more complex transistors into the same amount of space, the potential for quality problems increases dramatically. The cost of detecting and remediating these issues has also soared, relative to the actual cost of manufacturing. This has a direct bearing on profitability.

Two factors are primarily responsible for heightened quality risk: Increased cycle time and faster machine throughput. Accenture Strategy found that the requirements for manufacturing "advanced technology nodes" have more than doubled from approximately 34 to 75 mask layers since 2005. At an assumed 2 days per mask layer, this increases a company's exposure to quality incidents by nearly 500 percent (see Figure 3).[6]

The industry's current emphasis on quality control in the final stages of production is no longer sufficient to curb the increasing cost of quality. Companies can better manage costs and achieve the quality they need by identifying incidents earlier in the production cycle.

Figure 3. The number of wafers exposed to quality incidents has grown by a factor of five since 1995.

YEAR	# OF WAFERS EXPOSED TO END-OF-LINE QUALITY INCIDENTS
1995	92,400
2000	194,880
2005	448,800
2010	528,000
2015	725,760
2020	972,000

Source: Accenture Strategy analysis.

PUTTING MOORE'S LAW IN ITS PLACE

As they consider their growth strategies moving forward, semiconductor companies should adopt three principles to help balance the risks and opportunities that Moore's Law presents.

CHOOSE CAREFULLY. As R&D organizations continue to push the upper bounds of technology, they must do so with an understanding of manufacturing supply and availability. At the same time, semiconductor companies must think carefully about the costs, benefits and requirements of becoming an advanced node leader. This means carefully assessing product portfolios, manufacturing capabilities,

supply capacity, vendor relationships and, of course, costs. It also means understanding market opportunities and trends across a range of solutions.

What their assessments are likely to reveal is that there are a number of market opportunities for advanced technologies. But exploiting those opportunities can come at a high cost. Other markets, which are perfectly content with older nodes, may present sustained growth potential. A diverse product portfolio comprising both traditional and advanced node technologies is usually the best strategy. It increases the likelihood that semiconductor companies will achieve both the growth and profitability that competitiveness now requires.

LEVERAGE DESIGN CYCLES. With the cost of advanced node design steadily rising, it is critical that semiconductor companies generate as much value as possible from existing investments. If customers are not demanding ultra-dense nodes, there's little need to manufacture them. Instead, companies should continue producing older nodes for existing applications, "sweating" their current assets wherever possible.

Semiconductor companies should also develop a keen understanding of trends and requirements in other market segments to identify new, untapped opportunities. They should introduce new solutions that utilize the older technology. This is about squeezing as much value from IP as possible.

There will be scenarios in which it makes economic sense for semiconductor companies to move into advanced node manufacturing. In these instances, they should generate the greatest return on their investments, think ahead, and identify opportunities to shift the newer technology to other solutions or industries, as appropriate.

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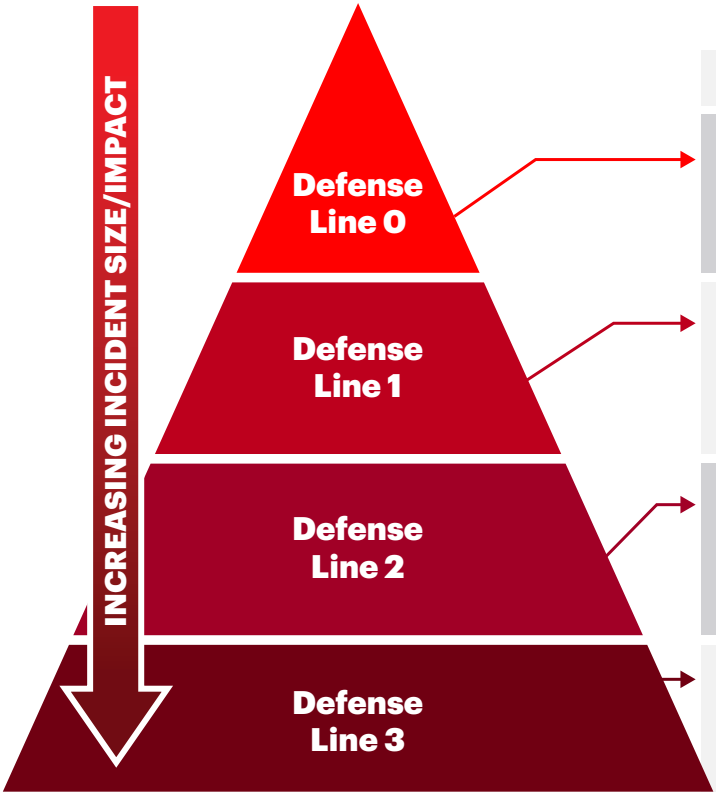
BE MORE VIGILANT. Traditionally, post-processing metrology and end-of-line measurements have been the most reliable indicators of quality during the chip-manufacturing process. However, post-processing metrology does not measure 100 percent of all products. It is based on a statistical sampling of material running through the line to establish high confidence that there are no quality issues. We believe companies must adapt their approach to process control so that incident detection moves up the value chain (see Figure 4).

Figure 4. Four defense lines to detect quality issues.



AREA	CHARACTERISTICS	EXAMPLES
During Processing	• Instant • 100% sample rate	• Tool errors
Post Processing	• Captured during wafer lot completion • 100% sample rate by lot average	• Average temperature • Processing time
Post Processing Metrology	• Measurement of product after process completion • Sample rate determined by engineering	• Critical dimensions • Layer thickness
End of the Line	• Test of final product • Sampling dictated by engineering	• Probe yield • Final test yield • Parametric data

Source: Accenture Strategy analysis.

With this model, each of the four stages acts as a quality check before the product moves on. Detecting issues at these four defense lines requires semiconductor companies and their ecosystem partners to share data. By establishing data-sharing mechanisms between companies at different stages in the semiconductor supply chain, companies will be able to leverage advanced data analytics capabilities to detect issues much earlier in the product lifecycle.

A NEW RACE

There is no doubt that semiconductor companies will continue to apply their resourcefulness, drive and creativity to keep pace with Moore's Law. But doubling wafer density no longer carries the advantages it once did.

In this high-cost/low-return environment, winners will set the rules of the race. No longer will they pursue new innovations simply because they can. They will pursue opportunities that are clearly aligned to a viable business strategy, as well as their growth and profitability objectives.

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NOTES

[1] Intel corporate site.

[2] Accenture Strategy analysis, 2017.

[3] Dr. Handel Jones (International Business Strategies), "Semiconductor Industry from 2015 to 2025," SEMI, August 4, 2015.

[4] "Technology Quarterly," The Economist, March 12, 2016.

[5] Accenture Strategy analysis, 2017.

[6] Ibid.

ABOUT ACCENTURE

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